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Terms used **static timing analysis sequential elements timing delay echo signal VLSI**

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81 Session 5A: Embedded tutorial: embedded software and systems: Low power system scheduling and synthesis

Niraj K. Jha

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(168.32 KB) Additional Information: full citation, abstract, references, citings, index terms

Many scheduling techniques have been presented recently which exploit dynamic voltage scaling (DVS) and dynamic power management (DPM) for both uniprocessors and distributed systems, as well as both real-time and non-real-time systems. While such techniques are power-aware and aim at extending battery lifetimes for portable systems, they need to be augmented to make them battery-aware as well. We will survey such power-aware and battery-aware scheduling algorithms. Also, system synthesis algorit ...

82 Session 8D: Timing and noise analysis: False-noise analysis using logic implications

Alexey Glebov, Sergey Gavrilov, David Blaauw, Supamas Sirichotiyakul, Chanhee Oh, Vladimir Zolotov

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(133.42 KB) Additional Information: full citation, abstract, references, citings, index terms

Cross-coupled noise analysis has become a critical concern in today's VLSI designs. Typically, noise analysis makes an assumption that all aggressing nets can simultaneously switch in the same direction. This creates a worst-case noise pulse on the victim net that often leads to false noise violations. In this paper, we present a new approach that uses logic implications to identify the maximum set of aggressor nets that can inject noise simultaneously under the logic constraints of the circuit. ...

83 Session 8D: Timing and noise analysis: On the signal bounding problem in timing analysis

Jin Fuw Lee, D. L. Ostapko, Jeffery Soreff, C. K. Wong

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(160.52 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we study the propagation of slew dependent bounding signals and the corresponding slew problem in static timing analysis. The selection of slew from the latest arriving signal, a commonly used strategy, may violate the rule of monotonic delay. Several methods for generating bounding signals to overcome this difficulty are described. The accuracy and monotonicity of each method is analyzed. These methods can be easily implemented in a static timer to improve the accuracy.

84 Session 8D: Timing and noise analysis: A symbolic simulation-based methodology for generating black-box timing models of custom macrocells

Clayton B. McDonald, Randal E. Bryant

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(110.81 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a methodology for generating black-box timing models for full-custom transistor-level CMOS circuits. Our approach utilizes transistor-level ternary symbolic timing simulation to explore the input arrival time space and determine the input arrival time windows that result in proper operation. This approach integrates symbolic timing simulation into existing static timing analysis flows and allows automated modelling of the timing behavior of aggressive full-custom circuit design styles ...

85 A VLSI-Based Model of Azimuthal Echolocation in the Big Brown Bat

Timothy Horiuchi, Kai M. Hynna

November 2001 **Autonomous Robots**, Volume 11 Issue 3

Full text available: Publisher Site Additional Information: full citation, abstract

The azimuthal localization of objects by echolocating bats is based on the difference of echo intensity received at the two ears, known as the interaural level difference (ILD). Mimicking the neural computation of ILD in bats, we have constructed a spike-based VLSI model of the lateral superior olive (LSO) that can successfully produce direction-dependent responses. This simple algorithm, while studied in the acoustic domain, is applicable to any localization based on direction-dependent sign ...

Keywords: azimuthal echo localization, spiking neural model

86 Static timing analysis

Yuji Kukimoto, Michel Berkelaar, Karem Sakallah

November 2001 **Logic Synthesis and Verification**

Additional Information: full citation, abstract, references, index terms

Static timing analysis is a technique for estimating the delay of a design without electrical simulation. It is widely adopted in industry for timing verification and optimization. This chapter will overview the basics of static timing analysis.

87 Modeling and minimization of interconnect energy dissipation in nanometer technologies

Clark N. Taylor, Sujit Dey, Yi Zhao

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(76.31 KB) Additional Information: full citation, abstract, references, citings, index terms

As the technology sizes of semiconductor devices continue to decrease, the effect of nanometer technologies on interconnects, such as crosstalk glitches and timing variations, become more significant. In this paper, we study the effect of nanometer technologies on

energy dissipation in interconnects. We propose a new power estimation technique which considers DSM effects, resulting in significantly more accurate energy dissipation estimates than transition-count based methods for on-chip ...

88 Static timing analysis including power supply noise effect on propagation delay in VLSI circuits
Geng Bai, Sudhakar Bobba, Ibrahim N. Hajj
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(242.00 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents techniques to include the effect of supply voltage noise on the circuit propagation delay of a digital VLSI circuit. The proposed methods rely on an input-independent approach to calculate the logic gate's worst-case power supply noise. A quasi-static timing analysis is then applied to derive a tight upper-bound on the delay for a selected path with power supply noise effects. This upper-bound can be further reduced by considering the logic constraints and dependencies ...

89 Low-energy intra-task voltage scheduling using static timing analysis
Dongkun Shin, Jihong Kim, Seongsoo Lee
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(113.20 KB) Additional Information: full citation, abstract, references, citings, index terms

We propose an intra-task voltage scheduling algorithm for low-energy hard real-time applications. Based on a static timing analysis technique, the proposed algorithm controls the supply voltage within an individual task boundary. By fully exploiting all the slack times, a scheduled program by the proposed algorithm always complete its execution near the deadline, thus achieving a high energy reduction ratio. In order to validate the effectiveness of the proposed algorithm, we built a softwa ...

90 A new gate delay model for simultaneous switching and its applications
Liang-Chi Chen, Sandeep K. Gupta, Melvin A. Breuer
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(163.26 KB) Additional Information: full citation, abstract, references, citings, index terms

91 Functional correlation analysis in crosstalk induced critical paths identification
Tong Xiao, Malgorzata Marek-Sadowska
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(60.06 KB) Additional Information: full citation, abstract, references, citings, index terms

In deep submicron digital circuits capacitive couplings make delay of a switching signal highly dependent on its neighbors switching times and switching directions. A long path may have a large num-ber of coupling neighbors with difficult to determine interdepen-dencies. Ignoring the mutual relationship among the signals may result in a very pessimistic estimation of circuit delay. In this paper, we apply efficient functional correlation analysis techniques to identify critical paths caused ...

92 Design of robust global power and ground networks
S. Boyd, L. Vandenberghe, A. El Gamal, S. Yun
April 2001 **Proceedings of the 2001 international symposium on Physical design**

Full text available: pdf(225.62 KB) Additional Information: full citation, abstract, references, citings, index terms

We consider the problem of determining optimal wire widths for a power or ground network, subject to limits on wire widths, voltage drops, total wire area, current density, and power dissipation. To account for the variation of the current demand, we model it as a random vector with known statistics, possibly including correlation between subsystem currents. Other researchers have shown that when the variation in the current is not taken into account, the optimal network topology is a tree. ...

Keywords: convex optimization, interconnect sizing, power and ground network design

93 Analysis and optimization of thermal issues in high-performance VLSI

Kaustav Banerjee, Massoud Pedram, Amir H. Ajami

April 2001 **Proceedings of the 2001 international symposium on Physical design**

Full text available: pdf(320.70 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper provides an overview of various thermal issues in high-performance VLSI with especial attention to their implications for performance and reliability. More specifically, it examines the impact of thermal effects on both interconnect design and electromigration reliability and discusses their impact on the allowable current density limits. Furthermore, it also discusses how thermal and reliability constrained current density limits may conflict with those obtained through purely p ...

94 An effective low powr design methodology based on interconnect prediction

Shih-Hsu Huang

March 2001 **Proceedings of the 2001 international workshop on System-level interconnect prediction**

Full text available: pdf(150.24 KB) Additional Information: full citation, abstract, references, index terms

The demand for low power digital systems has motivated significant research. However, the power estimation at the logic level is a difficult task because interconnect plays a role in determining the total chip power dissipation. As a result, the power optimization at the logic level may be inaccurate due to the lack of physical place and route information. In this paper, we will present an effective low power design methodology based on interconnect prediction at the logic level. The propos ...

95 A statistical static timing analysis considering correlations between delays

Shuji Tsukiyama, Masakazu Tanaka, Masahiro Fukui

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: pdf(66.13 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a new algorithm for the statistical static timing analysis of a CMOS combinatorial circuit, which can treat correlations of arrival times of input signals to a logic gate and correlations of switching delays in a logic gate. We model each switching delay by a normal distribution, and use a normal distribution of two stochastic variables with a coefficient of correlation for computing the distribution of output delay of a logic gate. Since the algorithm takes the co ...

96 Design technology productivity in the DSM era (invited talk)

Andrew B. Kahng

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: pdf(126.72 KB) Additional Information: full citation, abstract, references, index terms

Future requirements for design technology are always uncertain due to changes in process technology, system implementation platforms, and applications markets. To correctly identify the design technology need, and to deliver this technology at the right time, the design technology community - commercial vendors, captive CAD organizations, and academic researchers - must focus on improving design technology time-to-market and quality-of-result. Put another way, we must address the well-known ...

97 Catastrophic Short and Open Fault Detection in Bipolar CML Circuits: A Case Study
André Ivanov, Vikram Devdas
December 2000 **Journal of Electronic Testing: Theory and Applications**, Volume 16 Issue 6

Full text available: Publisher Site Additional Information: full citation, abstract, index terms

The detection of catastrophic short and open faults in bipolar *current mode logic* (CML) circuits is studied. The non-intrusive tests considered include functional (logic) tests, an I_{dd} test, and a *common-mode test*. A 622 Mbps SONET SIPO (Serial-In/Parallel-Out) and a PISO (Parallel-In/Serial-Out) circuit form the basis of this case study.

Keywords: CML circuit testing, bipolar circuit testing, catastrophic fault detection, current mode logic (CML), defect-based testing

98 Session 8A: static timing analysis: Transistor-level timing analysis using embedded simulation
Pawan Kulshreshtha, Robert Palermo, Mohammad Mortazavi, Cyrus Bamji, Hakan Yalcin
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(86.18 KB) Additional Information: full citation, abstract, references

A high accuracy system for transistor-level static timing analysis is presented. Accurate static timing verification requires that individual gate and interconnect delays be accurately calculated. At the sub-micron level, calculating gate and interconnect delays using delay models can result in reduced accuracy. Instead, the proposed method calculates delays through numerical integration using an embedded circuit simulator. It takes into account short circuit current and carefully chooses the se ...

99 Session 8A: static timing analysis: Slope propagation in static timing analysis
David Blaauw, Vladimir Zolotov, Savithri Sundareswaran, Chanhee Oh, Rajendran Panda
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(116.13 KB) Additional Information: full citation, abstract, references, citings

Static timing analysis has traditionally used the PERT method for identifying the critical path of a digital circuit. Due to the influence of the slope of a signal at a particular node on the subsequent path delay, an earlier signal with a signal slope greater than the slope of the later signal may result in a greater delay. Therefore, the traditional method for timing analysis may identify the incorrect critical path and report an optimistic delay for the circuit. We show that the circuit delay ...

100 Session 8A: static timing analysis: Switching window computation for static timing analysis in presence of crosstalk noise
Pinhong Chen, Desmond A. Kirkpatrick, Kurt Keutzer
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on**

Computer-aided design

Full text available: pdf(88.18 KB) Additional Information: full citation, abstract, references, citings

Crosstalk effect is crucial for timing analysis in very deep submicron design. In this paper, we present and compare multiple scheduling algorithms to compute switching windows for static timing analysis in presence of crosstalk noise. We also introduce an efficient technique to evaluate the worst case alignment of multiple aggressors.

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